

ABSTRACT OF THE DISCLOSURE

A digital filter having a first plurality of delay components connectable in series and having an input and an output and a second plurality of delay components connectable in series and having an input and said output. A system input is coupled to each of the inputs of the first and second pluralities of delay components. A plurality of adders is provided, each adder couplable alternately to a different delay component of the first plurality of delay components and then to a different delay component of the second plurality of delay components. The number of delay components of the second plurality of delay components is equal in number to the first plurality of delay components. The system input can be concurrently coupled to each of the inputs of the first and second pluralities of delay components. In accordance with a first embodiment of the invention, the number of adders is equal to one less than the number of delay components in first or second pluralities of delay components. In accordance with a second embodiment of the invention, the number of adder is equal to the number of delay components in the first or second pluralities of delay components. The digital filter is preferably a FIR